

Preface

During the four years since the RISC System/6000® (RS/6000) announcement in February of 1990, IBM® has strengthened its product line with microprocessor enhancements, increased memory capacity, improved graphics, greatly expanded I/O adapters, and new AIX® and compiler releases. In 1991, IBM began planning for future RS/6000 systems that would span the range from small, battery-operated products to very large supercomputers and mainframes. As the first step toward achieving this "palmtop to teraFLOPS" goal with a single architecture, IBM investigated further optimizations for the original POWER Architecture™. This effort led to the creation of the PowerPC™ alliance (IBM Corporation, Motorola™, Inc., and Apple® Computer Corporation) and the definition of the PowerPC Architecture™. Today, the single-chip PowerPC 601™ processor is the basis of IBM's entry systems. A more aggressively superscalar version of the original POWER processor, the multichip POWER2™ processor, is exploited in our current IBM high-end RISC systems. As technology continues to advance, PowerPC implementations will provide the basis for high-performance 64-bit super servers.

This special issue of the *IBM Journal of Research and Development* focuses on the POWER2 and PowerPC portions of IBM's wide-ranging announcement in late 1993. The new POWER2 processor nearly doubles the performance of the earlier high-end models. The PowerPC 601 processor was introduced in the RISC System/6000 Model 250, the first system in the industry to use the PowerPC Architecture created by the strategic IBM/Motorola/Apple alliance. These workstations achieved industry-leading performance and price/performance on virtually every industry-standard benchmark, including SPECint92™, SPECfp92™, Linpack, TPP, TPC-A™, and TPC-C™. Compared to the 1990 offerings, SPEC performance nearly quadrupled, transaction performance improved by a factor of almost five, maximum memory capacity quadrupled, and the maximum disk capacity grew by an order of magnitude.

The POWER2 design exploits both multichip technology and a larger die size to execute up to six instructions (eight operations) per clock cycle. Many of the higher-performance POWER2-based systems provide peak execution rates in excess of a half billion operations per second. The paper by White and Dhawan provides an overview of the POWER2 design. Shippy and Griffith describe the dual fixed-point unit design, the data cache unit, and the storage control unit. Hicks, Fry, and Harvey explain the dual floating-point unit design. Barreh et al. describe hardware strategies to minimize compare-branch penalties in the instruction cache unit.

Welbon et al. discuss a POWER2 hardware performance-monitoring facility which provides execution

characteristics that can identify opportunities for application performance improvement. This facility can also be used to gather information crucial to future design decisions.

Two performance papers conclude the POWER2 portion of this issue. Franklin et al. analyze some of the key POWER2 hardware contributions to performance on the commercial workloads. Agarwal, Gustavson, and Zubair relate their experiences with optimizing the high-performance Engineering/Scientific Subroutine Library (ESSL) for the POWER2 implementation.

While POWER2 and PowerPC implementations provide the opportunity for high-performance systems, optimizing software is also key in delivering end-user performance. Blainey discusses aspects of the TOBEY compiler, with special emphasis on instruction scheduling for the RS/6000 products. Heisch describes TDPR, a prototype version of FDPR, a program restructuring tool which improves application performance by placing frequently executed code blocks so as to minimize instruction cache misses and branch penalties.

IBM and the PowerPC alliance are currently developing a family of five PowerPC designs. IBM and Motorola designers at the Somerset Design Center in Austin will optimize single-chip implementations of the PowerPC Architecture for high-volume products. The high-end requirements of the large server and workstation products will be addressed with multichip PowerPC implementations from IBM.

IBM entry-level workstation products introduced the PowerPC 601 microprocessor, the first member of the PowerPC family. The goal for the PowerPC 601 designers was to quickly bring PowerPC to the market. Vaden et al. describe the microarchitecture and performance aspects of the PowerPC 601 processor. Brodnax et al. discuss the PowerPC 601 circuitry and chip implementation details. Future products are planned that will incorporate the PowerPC 603™, PowerPC 604™, and the 64-bit PowerPC 620™ implementations as they become available. In addition, the price and price/performance of the PowerPC family enable lower-cost "RISC PCs" to be built using PowerPC microprocessors. These "RISC PCs" will be developed by the IBM POWER Personal Systems Division.

The PowerPC and POWER2 systems signify a major milestone in IBM's commitment to the "palmtops to teraFLOPS" strategy. The PowerPC 601 chip extends the entry products further into the high-volume market by providing exceptional performance in a low-cost single-chip microprocessor. The high-end POWER2 implementation extracts the maximum performance achievable in today's technology, thrusting the IBM RISC processors into the supercomputing and large-server environments. IBM POWER Parallel Systems extends the RS/6000 processing

capability by providing IBM POWER Parallel SP2™ systems with up to 512 POWER/POWER2 nodes. In addition to scalability, four-way High Availability Cluster Multi-Processor (HACMP) systems provide the reliability/availability that one would expect from mainframe-class systems by supporting a "no single point of failure" capability, even when one processor is off line. This impressive base of processing technology complements a commitment to high-performance compilers and strong graphics offerings.

This robust product line addresses the cost-driven requirements of the entry workstation market, the transaction and server requirements of the commercial market, and the computation-intensive requirements of the technical market. These hardware offerings result from a team effort by many dedicated and talented individuals from around the world. Their expertise and skill in a wide range of disciplines were key to achieving this significant step toward the goal of a comprehensive architecture. We want to thank all those involved in continuing the success of the RISC System/6000 line.

Phil D. Hester
Vice President
RISC System/6000 Division

Bill Filip
IBM Vice President and President
RISC System/6000 Division